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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,827	10/01/2003	Kiyoshi Yoneda	492322013800	8768

25227 7590 02/14/2007

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EXAMINER	
XIAO, KE	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,827	YONEDA, KIYOSHI	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 10* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (US 5,990,629).

Regarding independent **Claim 1**, Yamada teaches an electro luminescent display device (Yamada, Fig. 1), comprising:

a plurality of pixels (Yamada, Fig. 1);

an electroluminescent element provided in each of the pixels (Yamada, Fig. 1 element 11);

a pixel selecting transistor provided in each of the pixels and selecting a corresponding pixel in response to a gate signal (Yamada, Fig. 1 element 13); and

a driving transistor provided in each of the pixels, supplying an electric current to a corresponding electroluminescent element in response to a display signal supplied through the corresponding pixel selecting transistor (Yamada, Fig. 1 element 12),

wherein the pixel selecting transistor comprises an active layer made of polysilicon, and the driving transistor comprises an active layer made of amorphous silicon (Yamada, Col. 7 lines 25-55).

Regarding independent **Claim 2**, Yamada teaches an electro luminescent display device (Yamada, Fig. 1), comprising:

a plurality of pixels (Yamada, Fig. 1);

an electroluminescent element provided in each of the pixels (Yamada, Fig. 1 element 11);

a pixel selecting transistor provided in each of the pixels and selecting a corresponding pixel in response to a gate signal (Yamada, Fig. 1 element 13); and

a driving transistor provided in each of the pixels, supplying an electric current to a corresponding electroluminescent element in response to a display signal supplied through the corresponding pixel selecting transistor (Yamada, Fig. 1 element 12),

wherein a carrier mobility of the driving thin film transistor is lower than a carrier mobility of the pixel selecting thin film transistor (Yamada, Col. 7 lines 25-55). To elaborate Yamada shows that the selecting transistor is based on polysilicon and the driving transistor is based on amorphous silicon and it is well known in the art that amorphous silicon has lower carrier mobility than polysilicon.

Regarding **Claim 10**, Yamada further teaches that the pixel selecting transistor does not include any amorphous silicon (Yamada, Col. 7 lines 25-55). To elaborate Yamada teaches that the pixel selecting transistor can be either amorphous or

polysilicon which means that when it is made up of polysilicon it does not include any amorphous silicon as claimed.

Allowable Subject Matter

Claims 3 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding **Claim 3**, prior art fails to teach the combination of "the pixel selecting thin film transistor comprises a first polysilicon active layer and the driving thin film transistor comprises a second polysilicon active layer" and "a carrier mobility of the driving thin film transistor is lower than a carrier mobility of the pixel selecting thin film transistor" as recited from independent Claim 2 from which Claim 3 depends.

Regarding **Claim 4**, it depends directly from Claim 3.

Response to Arguments

Applicant's arguments filed December 19th, 2006 have been fully considered but they are not persuasive.

Regarding Claims 1 and 2, the applicant argues that Yamada fails to teach that the selecting transistor comprises an active layer made of polysilicon and the driving transistor comprises an active layer made of amorphous silicon thereby the driving thin film transistor has a lower carrier mobility than the pixel selecting thin film transistor. The examiner respectfully disagrees. To elaborate the applicant contends that no part of Yamada requires the semiconductor layers the driving transistor and selecting transistors to be different, however it also doesn't require them to be the same. Yamada clearly states that either one of the semiconductor layers can be made up of either amorphous or polysilicon, and such a teaching is inclusive of the teaching that the selecting TFT is made of polysilicon and the driving TFT is made of amorphous silicon as claimed. The examiner also notes that it is an inherent characteristic of TFTs that amorphous based TFTs have lower mobility than polysilicon TFTs of otherwise similar characteristics therefore the limitations of Claim 2 are also satisfied. Finally the applicant argues that Yamada does not provide a manufacturing process to support the creation both amorphous and polysilicon layers. It is noted by the examiner that the specific manufacturing process is not claimed and therefore has no bearing on the claimed subject matter or the rejection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571) 272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

February 6th, 2006 - kx-

SUPERVISORY PATENT EXAMINER